Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_

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**End Semester Examination – Nov/Dec – 2018**

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| **Code :** | **14EC2069** | **Duration :** | **3hrs** |
| **Sub. Name :** | **VLSI DESIGN** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | With neat diagram, illustrate in detail about Si-gate NMOS process. | CO1 | 12 |
| b. | Discuss in detail about full custom design and list its advantages. | CO3 | 8 |
| (OR) | | | | |
| 2. | a. | Explain the different fabrication steps of Silicon On Insulator (SOI) process and list the advantages of SOI process. | CO1 | 12 |
| b. | Distinguish about the different types of Gate array Layout. | CO1 | 8 |
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| 3. | a. | Explain NMOS enhancement mode transistor region of operation for various terminal voltages. | CO1 | 12 |
| b. | Construct small signal model for an MOS transistor, and evaluate the small signal AC characteristics. | CO1 | 8 |
| (OR) | | | | |
| 4. | a. | Show the relationship between Drain-to-source current (Ids) Vs Vds in non-saturation and saturation region and find the drain current in cutoff, non saturation and saturation region. | CO1 | 12 |
| b. | Discuss in detail about channel length modulation, threshold voltage variation, Drain punch through and Hot electron effect of MOS transistor. | CO1 | 8 |
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| 5. | a. | Design CMOS logic for the following functions:  Z=(A.B) + C.(D+E)  Z=((A.B)+C).D | CO3 | 10 |
| b. | With neat diagram explain in detail about NMOS Layout design rules. | CO2 | 10 |
| (OR) | | | | |
| 6. | a. | Construct the circuit, stick diagram and layout of 2-input CMOS NOR Gate. | CO2 | 8 |
| b. | Elaborate n-well based CMOS Layout design rules. | CO2 | 12 |
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| 7. | a. | Show the layers and color coding in NMOS process and construct the circuit and stick diagram of NMOS NAND Gate | CO2 | 10 |
| b. | Illustrate in detail about Dynamic CMOS logic and design the following Boolean expression using Dynamic CMOS Logic.  F=(A1.A2.A3)+(B1.B2) | CO2 | 10 |
| (OR) | | | | |
| 8. | a. | Explain in detail about CMOS Domino logic and design the following expression using the same.  (Z= A.B+ C.D) | CO2 | 12 |
| b. | Design Z=((A.B.C)+D) using pseudo NMOS logic. | CO3 | 8 |
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|  | | **Compulsory**: |  |  |
| 9. | a. | Design 3-input NAND gate using Dynamic CMOS logic. | CO2 | 8 |
| b. | With neat diagram explain in detail about **clocked CMOS** logic (C2MOS) and design 3-input NAND gate using **clocked CMOS** (C2MOS) logic. | CO2 | 12 |